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(54) **THIN FILM TRANSISTOR AND ITS MANUFACTURE**

electrodes 12a, 12b are made to overlap with the position and shape of the channel region 17 in plan view.

(57) Abstract:

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PROBLEM TO BE SOLVED: To reduce capacitance between a pair of gate electrodes and source/drain regions, by forming the pair of gate electrodes on the top and bottom surfaces of a semiconductor thin film to sandwich a channel region comprising the semiconductor thin film between them, and by making their positions and shapes overlap with the position and shape of the channel region in plan view.

SOLUTION: Forming a first gate electrode 12a on an insulation substrate 11, a first gate insulation film 13a such as a silicon oxide film is formed on the whole surfaces of the gate electrode 12a and insulation substrate 11. Forming thereon a semiconductor thin film, source/drain regions 15, 16 are formed in both side end regions of the semiconductor thin film to form a channel region 17 between the regions 15, 16. Further, forming a second insulation film 13b on the whole surface of the region including the semiconductor thin film, a second gate electrode 12b is formed thereon. Hereupon, the positions and shapes of the first and second gate

